Sub-Threshold Adiabatic Logic for Low Power Applications

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Abstract: Digital sub-threshold logic circuits can be used for applications in the ultra-low power end of the design spectrum, where performance is of secondary importance. A sub-threshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current. This minute leakage current, however, limits the maximum performance at which the sub-threshold circuit can be operated. Sub-threshold CMOS theory is a technique which can reduce the power consumption to lower than threshold voltage specified and adiabatic logic circuit is a technique to reduce energy consumption by suppressing the voltage applied to the resistance of the circuit. This paper proposes that sub-threshold adiabatic logic design implementation of carry look ahead adder. The simulation result is done in Tanner EDA Tool using 22nm technology.

Keywords: RFID, CMOS, EDA, SAL.

I. INTRODUCTION

Power consumption is rapidly becoming a limiting factor in integrated circuit technology as device sizes shrink. Applications such as wireless sensors, RFID tags, and similar devices have only a very small amount of power available to them, and must be designed to use a minimum of energy. Computer processors have massive amounts of power available, but can fail or become permanently damaged if the energy they dissipate causes severe heating. In an attempt to address these concerns, we have tested the effectiveness of two low-power techniques, sub-threshold biasing and adiabatic charging; in the design the continuous growth of recent mobile and portable devices and applications has caused a tremendous thrust for low power circuit design. Various methods and techniques, such as voltage scaling, clock gating, etc. have been applied successfully in the medium power, medium performance region of the design spectrum for lower power consumption. Nevertheless, in some applications where ultra-low power consumption is the primary requirement and performance is of secondary importance, a more aggressive approach is warranted. Operating the transistors of a digital logic in the sub- threshold region has recently been proposed to achieve ultra- low power consumption. A sub-threshold digital circuit manages to satisfy the ultra-low power requirement because it uses the leakage current as its operating switching current. This minute leakage current, however, limits the maximum performance at which the sub-threshold circuit can be operated. The sub-threshold circuit is thus suitable for certain applications which do not require very high performance. In this paper we designed the logic gates in SAL logic technique. Later, we apply this technique to design a 4-bit CLA unit and compared between the conventional design and the proposed SAL logic was shown in below sections

II. ADIABATIC PRINCIPLE

The operation of adiabatic logic gate is divided into two distinct stages: one stage is used for logic evaluation; the other stage is used to reset the gate output logic value. Both the stages utilize adiabatic switching principle. In the following section conventional switching and adiabatic switching analyzed in detail. Conventional switching there are three major sources of power dissipation in digital CMOS circuits those are dynamic, short circuit and leakage power dissipation. The dominant component is dynamic power dissipation and is due to charging, discharging of load capacitance. The equivalent circuits of CMOS logic for

charging and discharging.

A. Sub-Threshold Biasing

The concept of sub-threshold is fairly simple to understand, though the physics behind it can be daunting. In traditional CMOS processes the voltage threshold is the value for which the transistor is off. If the voltage potential from the transistors drain to source is below the threshold voltage this concept of the device being off is still considered true. However, in reality the transistor still retains it on off abilities at these low levels, because the current doesn't completely shut off, it is diminished exponentially. Though the transistor will not perform at the level it was designed for it will still operate similarly. We will show how our circuit performed with different VDD values set below the voltage threshold.

III. CMOS BASED CARRY LOOK AHEAD ADDER

Carry look-ahead uses a tree structure to parallelize carry generation. The tree structure is based on two intermediate signals the, "carry propagate" and the "carry generate". If the generate signal at a position is asserted, there is an unconditional carry out at that position, i.e. a carry is "generated" at that point. If the propagate is asserted, the carry out follows the carry in, i.e. a carry is "propagated" though that circuit. Carry look-ahead is shown in Fig.1. When units creating generate and propagate signals are combined into groups, like in Fig, The generate for the group is asserted if any unit has it's generate asserted and all subsequent propagates are asserted. The group propagate is asserted if all unit propagates are asserted. Most other arithmetic operations, e.g. multiplication and division are implemented using several add/subtract steps. Thus, improving the speed of addition will improve the speed of all other arithmetic operations. Accordingly, reducing the carry propagation delay of adders is of great importance. Different logic design approaches have been employed to overcome the carry propagation problem. One widely used approach employs the principle of carry look-ahead solves this problem by calculating the carry signals in advance, based on the input signals. This type of adder circuit is called as carry look-ahead adder (CLA adder). It is based on the fact that a carry signal will be generated in two cases:

- When both bits Ai and Bi are 1, or
- When one of the two bits is 1 and the carry-in (carry of the previous stage) is 1.

The carry-look ahead is a fast adder designed to minimize the delay caused by carry propagation in basic adders. It utilizes the fact that, at each bit position in the addition, it can be determined if a carry with be generated at that bit, or if a carry will be propagated. To get more insight of operation, let us consider the following Boolean equations of the carry look ahead logic.

Pi = Ai XOR Bi Carry propagate Gi = Ai AND Bi Carry generate

Both carry propagate and generate signals depend only on the input bits and thus will be Valid after respective gate delays (XOR gate area and delay is far more than AND gate)

A. Subthreshold Adiabaticlogic with CLA Design

The design and analysis of SAL-based 4-bit CLA are given to point out the workability and therefore the practicability of the proposed logics. When validating the logical practicality, we implemented associate SAL-based primary cell library, consisting of common digital gates, like buffer/inverter, two- input and three-input functions, complicated gates, and special gates like Half and Full adder, that are necessary to implement the 4-bit CLA. The digital gates of

the library are developed at electronic transistor level using pulse kind offer voltage as mentioned within the Hence, 22-nm technology file is used in our transistor-level designs which guarantee the manufacturability of our designs under all normal conditions with favorable yields Previous section. These structures check either the pull-up or the pull-down network of the static standard logic. For instance, to implement a NAND or a NOR gate, merely the pull-up network may be placed between the provision clock and also the output load capacitors, whereas an AND or an OR gate may be enforced using the pull-down network between the provision clock and also the output load capacitors.

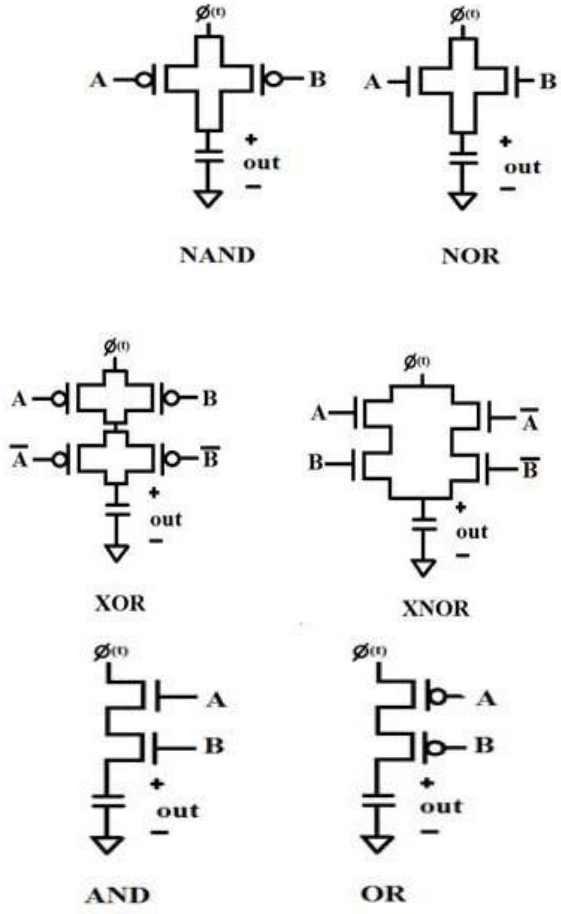


Fig.1. Carry look-ahead.

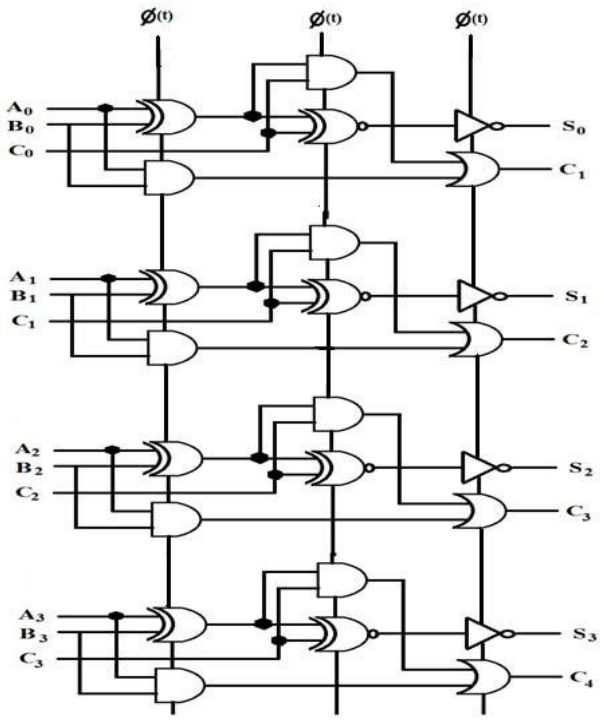
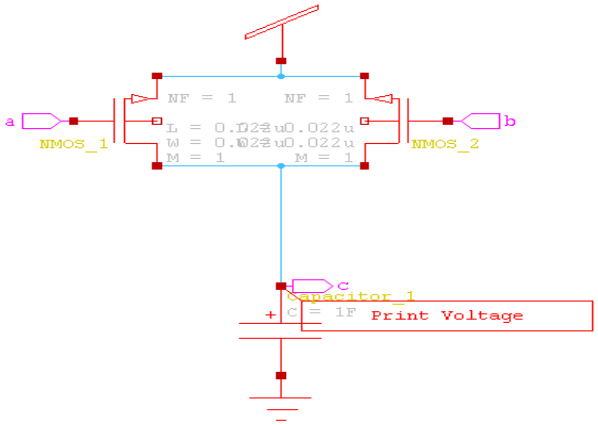


Fig.2.CLA Design.

Design and Analysis of Sub-Threshold Adiabatic Logic for Low Power Applications

Just in case of a NAND structure, for each input combination except A = B = 1, the output node voltage can follow the provision clock closely, and that we get an approximate output wave form. Once A = B = 1 through parallel pMOS junction transistor, run currents can flow because the transistors can behave nearly as a relentless current supply. A really touch of charge are keep across the load capacitor, i.e., rather than ground potential, terribly tiny voltage are across the output. The basic building block of 4- bit CLA is given in Fig.2 which is also very similar to the conventional structure. Hence, we implemented the sum (Si) in three stages to avoid delay mismatching with the carry generation. In SAL-based 4-bit CLA, every stage will be controlled by the supply clock. Like the conventional approach, the expression of the ith sum and the (i+ 1)th carry output.



IV. RESULTS

Fig.5.S- Edit design of SAL OR gate.

The design of conventional and the SAL logic gates are carried out using Tanner EDA tool. We show the simulation designs and graphs are shown below Figs.3 to 6.

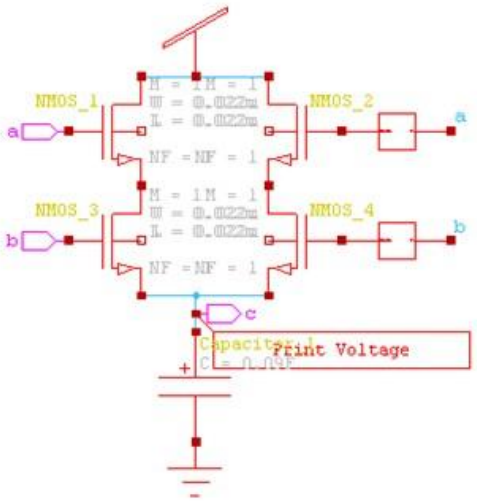


Fig.3. S-Edit Deign of SAL XNOR gate.

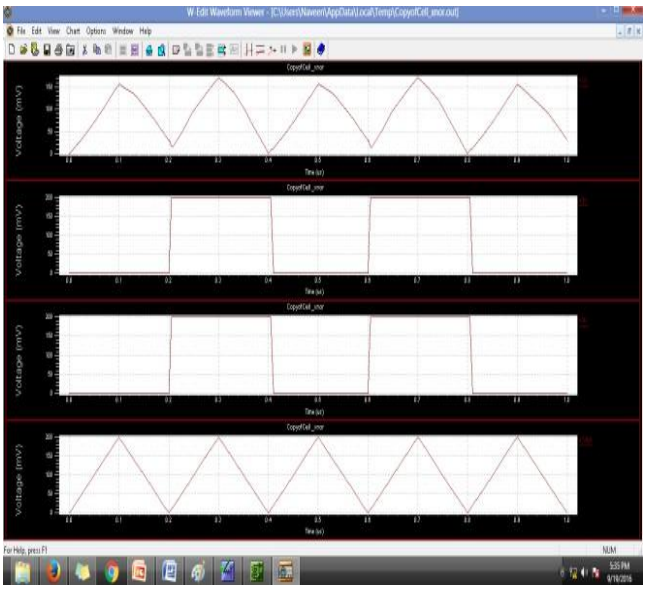


Fig.4.Simulation Waveform of SAL XOR Gate.

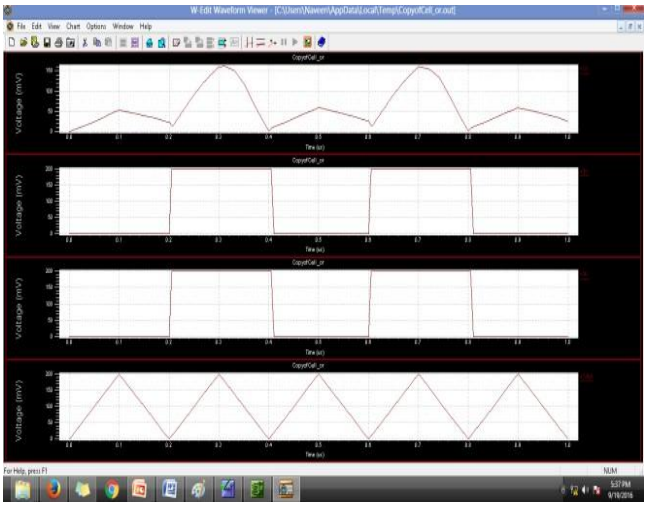


Fig.6. Simulation waveform of SAL OR gate.

TABLE I: Comparison of Conventional and Adiabatic CMOS Designs

Circuit	Convention Design	Adiabatic Design
Inverter	2.006633e-008 watts	2.423366e-010 watts
OR	1.274762e-008 watts	4.410477e-010 watts
AND	3.782368e-010 watts	8.437699e-011 watts
XOR	9.287881e-008 watts	2.318573e-009 watts
XNOR	1.779883e-008 watts	1.195571e-009 watts
CLA	3.633331e-008 watts	1.927558e-008 watts

V. CONCLUSION

SAL has been bestowed during this paper for the primary time within the literature to advance the ultralow power analysis. A closed form expression of the energy dissipation has been derived, from that insight is gained into the dependence of energy dissipation on style and method parameters. SAL saves considerable energy compared with the static standard logic counterpart over a large vary of frequency. Specifically, the impact of temperature variation on outpouring dissipation, output swing, etc., has been mentioned totally during this paper. Hence, the expected values of optimum frequency and optimum provide voltage virtually match the simulated ones. Post layout simulations mistreatment Tanner SPICE Spectra and The comparison with the static counterpart make a case for the work ability of SAL. This planned logic theme may be utilized in future energy-saving embedded circuits and chiefly for energy efficient devices wherever ultralow power and longevity area unit the pivotal problems.

VI. REFERENCE

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