Ways to Boost Your Synchronizer

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Abstract: Synchronizers are used to mitigate the effects of metastability in multiple clock domain system-on-chip devices. In order to enable reliable synchronization, the synchronizer MTBF (mean time between failures) should be much longer than the product lifetime. To achieve such high margins, multistage synchronizers are used. The most common synchronizer consists of a series of pipelined flip-flops. Several factors influence the performance of synchronizers: circuit design, process technology and operating conditions. Global factors apply to the entire integrated circuit, while others can be adjusted for each individual synchronizer in the design. Guidelines are provided to improve synchronizers: Avoiding scan and reset, selecting minimum size flip-flop cells, minimizing routing, minimum VTH and maximizing supply voltage.

Keywords: Metastability, MTBF, Multistage Synchronizers, Synchronization, Synchronizer, Tau Effective

I. INTRODUCTION

The system-on-chip (SOC) designer who wishes to use a synchronizer from a standard cell library would like to know the MTBF (Mean time between failures) of the system including the synchronizer before signing off on the design. Synchronizers play a key role in modern multiple clock system-on-chip (SoC) designs [1]. Such designs present thousands of clock domain crossings (CDC) where the system is prone to metastability errors. To mitigate those failures and ensure reliable signal transition between CDCs, synchronizers are used to convert domain timings. The type of synchronizer to be used for each is determined by the specific properties of the two clock domains involved. Different classifications of CDC have been studied. In [1][2],[3],[4] the classification of CDC is based on their frequency and phase relations, such as me- sochronous, plesiochronous and heterochronous. The latter group may be further sub-divided into ratiochronous and non-ratiochronous [5][6]. When there is no frequency and phase relationship, the clock domains are assumed mutually asynchronous. A different classification is based on clock sources [7]. Clocks are classified as non-coherent when they are sourced from different references and coherent when they share a common reference clock. The latter is the case when several phase locked loops (PLLs) are sourced from the same oscillator. For each category, specialized synchronizers have been developed to exploit the relationship and ensure correct operation improving performance and reliability.

In[8]-[12] synchronizers for mesochronous, plesiochronous and ratiochronous CDCs are proposed. The N-flip-flop synchronizer is usually employed in the asynchronous case [13]. The N-flip-flop synchronizer comprises a concatenated series of flip-flops as shown in Figure 1. This concatenated

flip-flop structure not only can be used as a standalone solution but it is also a central part in many other synchronizers such as FIFO synchronizers [14] and represents a critical part that has been studied intensively.

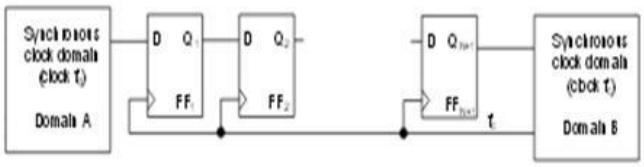
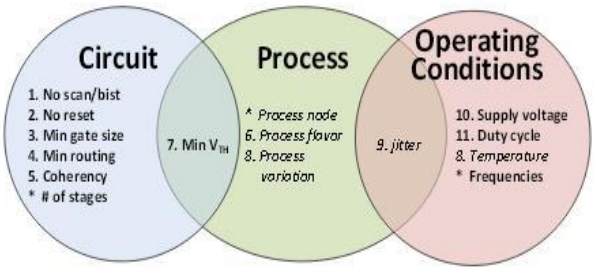


Fig1. A typical N-flip-flop synchronizer.

The designer that is to use concatenated flip-flops in her circuit is usually faced with questions about how many stages to use in the N-flip-flop synchronizer. The designer who wishes to use flip-flops from a standard cell library would like to know what the parameters are that influence the (Mean Time between Failures) of the system before signing off the design. This knowledge is increasingly valuable in nano-scale SoC designs because several factors have emerged that challenge the reliability of synchronizers. In particular, the required number of synchronizers in a design is growing rapidly; the variability of semiconductor parameters, as well as the sensitivity to operational conditions, has increased with scaling. Prediction of in depends on a variety of parameters, categorized as circuit parameters, process technology parameters and operating conditions parameters, as shown in Fig2. The Circuit considerations include questions such as what the necessary number of stages to include in the synchronizer is, as well as what the appropriate flip-flops to use in each stage. Placement and routing of the flips-flops in the pipeline is also classified as a circuit consideration. Process relates to the choice of technology node as well the process family and variability of each node. The selection of the threshold voltage of the transistors can be considered a process property, but since modern technologies allow mixing different threshold levels in the same design we consider it a circuit/process property and is presented in the intersection of both areas. Operating conditions are frequencies of the, supply voltages, duty cycle and temperature. Jitter is considered in between process and operating conditions because it is affected by both. This classification can be sub-divided into factors affecting metastability in a global or local way.



is determined by the number of flip-flops in the synchronizer. The larger the number of flip-flops the larger the resolution time allowed. Ignoring propagation and setup times, the resolution time is given by [14]

$$S = (N-1)\,TC \qquad (2)$$

Where N is the number of flip-flop stages and is the clock period of the receiving clock domain.

For each stage in the N-flip-flop synchronizer we consider a generalized flip-flop circuit, similar to the one shown in Fig3. The circuit comprises a master and a slave latch. Each one of these latches is characterized by a resolution time constant ($\tau i \in \{M, S\}$). The scheme in Figure 3 is an abstract scheme that serves as a framework and most flip-flop circuits are derivations of a similar form. We consider some of those derivations in the following sections.

Fig2. Classification of factors affecting meta- stability

Global factors affect all transistors in the design in the same way, while the effects of local factors may vary for different within the same IC. Local parameters are bolded in Fig2 while global ones are italicized. For global parameters we provide analytical insight on how they affect meta stability. For the local, we provide guidelines for how to choose the flip-flops forming the synchronizer and techniques that either improve reliability or prevent errors.

II. SYNCHRONIZATION FRAME WORK

In this section we describe the synchronization framework of the N-flip-flop synchronizer. The equations and derivations of this section form a common ground for subsequent sections. As stated above, most synchronizers include a N-flip-flop synchronizer comprising a pipeline of flip-flops. These concatenated flip-flops are designed to reduce the probability of synchronization failure. Generally, to reduce the probability of failures, the number of flip-flops in the pipe is increased. Increasing the number of stages increases resolution time which decreases the chance of metastable state at the subsequent logic. When the number of stages increases, latency through the pipeline increases reducing performance. Thus, latency is traded off for failure probability. Usually the probability of failure of the N-flip-flop synchronizer is measured by the mean time between failures (MTBF):

$$MTBF = \frac{e^{S/\tau}}{T_W \cdot F_C \cdot F_D}$$

Based on the resolution time constant for each latch in a flip-flop, the overall effective resolution time constant for the flip-flop is given by [21]

$$\tau_{eff} = \left(\frac{\alpha}{\tau_M} + \frac{(1-\alpha)}{\tau_S}\right)^{-1} \qquad (3)$$

$$g_m = g_{mn} + g_{mp} = \left(\mu_n C_{ox} \frac{W_n}{L} \frac{1}{1+\sqrt{a}} + \mu_p C_{ox} \frac{W_p}{L} \frac{\sqrt{a}}{1+\sqrt{a}}\right)(V_{DD} - |V_{THP}| - V_{THN})^{\alpha} \qquad (5)$$

III. BOOSTING SYNCHRONIZERS

This section describes eleven methods to improve the performance of synchronizers. The methods are divided into three categories, circuit, process and operating conditions, with each section containing the boosting methods for each category as described in Figure 2. Minimum threshold voltage (#7) lies in between circuit and process categories and is described in the process sub-section. Jitter (#9) lies between process and operating conditions category and is described in the operating conditions sub-section. Temperature, included in operating conditions, cannot be directly manipulated by the designer and hence its impact is included in the process variation sub-section (#8). The influence of factors marked by * in Figure 2 such as the number of stages, process node and frequencies are addressed in section II above. Since those parameters are included in
(1), their influence on is straightforward.

A. Boosting the Synchronizer Circuit

I. No Scan/BIST in synchronizer flip-flops

Scan is used in design-for-test (DFT) circuits. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in the integrated circuit. In general, a scan-enable pin is added to each flip-flop. When that signal is asserted, all flip-flops in the

design are connected in a long shift register. For this purpose, additional transistors are added to the standard flip-flop circuit. One example of such a circuit is shown in Figure 4 [17].

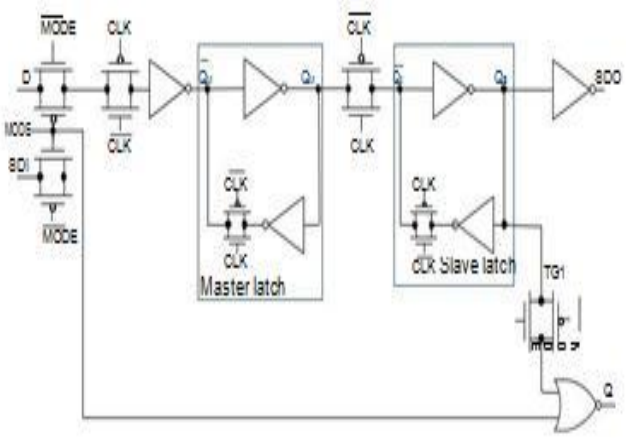


Fig4. Scan D-flip-flop with nor gate.

The scan path element receives its input either from the input or from the previous scan element via SDI. It is controlled by the scan-enable signal MODE, and the NOR gate is transparent when scan is disabled (MODE=0). The scan flip-flop presented is only one example of many derivatives and topologies existing in industry applications and academic publications. Other variants of scan flip-flops are presented in [18], [19]. Most of these configurations produce a negative effect on metastability resolution and induce an increase in T. In the circuit of Fig4, the capacitance of the metastable node of the slave latch (Q_s) is increased by the diffusion capacitances of the transmission gate (TG1), generating a higher T, according to (4). To demonstrate the effect quantitatively we simulated the circuit of Figure 3,

Figure 4 and [18]. Table I shows the results of circuit simulations confirming the increase in for the scan flip-flops examined. The table includes simulations for of master and slave latch and calculation of the effective of the flip-flop, following [11]. All T values are normalized to T_M of the circuit in Figure 3, and are simulated in functional rather than scan mode. The different flip-flop circuits do not affect the regeneration nature of the master latch and hence is almost the same in all flip-flops. However, the slave latch is affected by the scan transmission gate and SDO inverter, significantly increasing both and the resulting effective of the flip-flop. The increase in τ_S for the circuit of Fig4 with respect to Fig3 induces a significant decrease in MTBF.

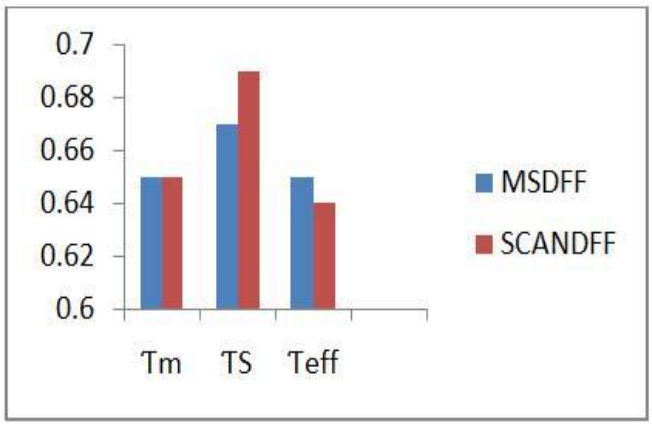


Fig5. Normalised T in scan flip-flops.

In summary, the use of flip-flops with scan capabilities has many benefits for IC test and quality control. However those benefits usually increase the effective capacitance in metastable prone latches, increasing T and reducing synchronizer MTBF. Thus, we

recommended avoiding the use of flip-flops with scan capabilities in synchronozers when possible.

II. No Reset in synchronizer flip-flops

Another topology frequently available in flip-flops is the use of asynchronous reset. The main advantage of this technique is to force the circuit into a known state in order to initialize hardware. There exist many different circuits that implement reset. One implementation of such a circuit is presented in Figure 6. When the flip-flop is reset (RST = 0),

the N-type transistor discharges node Q_{MBAR}, setting Q_{MBAR} = 0, QM = 1, and the node QS is charged through the P-type

transistor setting Q_S= 0, and Q = 0. The two reset transistors add parasitic capacitances to nodes Q_{MBAR} and $Q_{SBAR,}$ and, following (4), increase T for both the master and the slave latches of the flip-flop. Table II provides simulation results comparing for the circuits of Figure 3 and Figure 7. The results confirm the prediction that the reset transistors induce an increase in both T_M and T_S. In other circuit implementations of asynchronous or synchronous reset, this increment may be more pronounced. In summary, the use of asynchronous reset needs to be considered by the designer. The impact on synchronizer flip-flops needs to be evauated. To achieve a minimum T, asynchronous reset should be avoided.

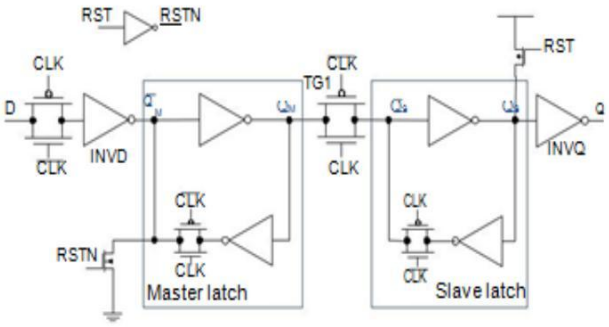
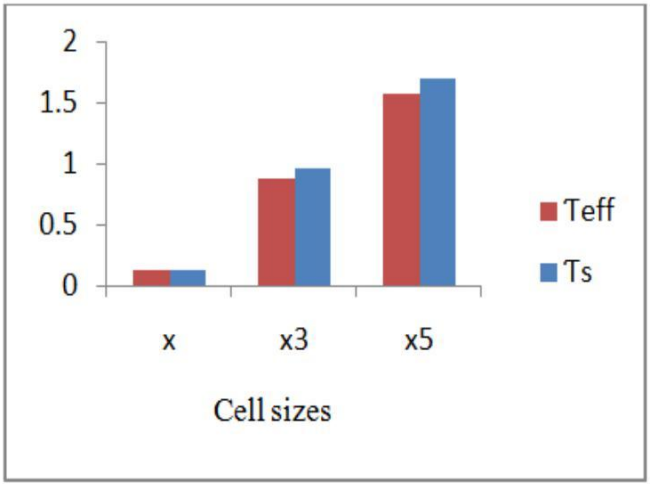


Fig6. Flip-flop with asynchronous reset.



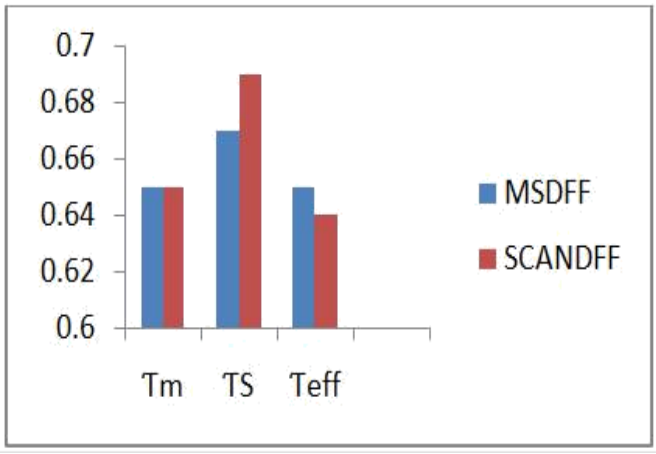


Fig7. Normalised T in reset flip-flops.

III. Minimum flip-flop cell size

One of the challenges facing the design engineer is to determine which flip-flop cell size from the available library to use in the synchronizer. According to (4), is affected by both the capacitance of the latch and its transconductance. Increasing gate size will increase both its capacitance and its g_m. In a first order approximation both changes cancel out and the value of T remains unchanged. Second order effects, especially the external load connected to the latch, should be considered to determine appropriate sizing. If the designer can determine the size of the each transistor inside the library flip-flop, then the loads on each latch should be chosen small in order to decrease T. For the circuit of Figure 3, that would imply reducing the size of transistors of transmission gate TG1 and inverter INVD for the master latch and TG1 and inverter INVQ for the slave latch. However, in general the designer cannot directly affect the sizing of the internal inverters in the flip-flop but has to choose from a pre-defined list of sizes that represent a general measure for the cell size. In most digital libraries, the differently sized flip-flop cells are optimized so that they handle different fan-out loads without drastically increasing the delay of the flip-flop. This is generally achieved by increasing the size of the output stage inverter (INVQ) for the different cell sizes. The internal portions of the flip-flops, however, are typically unchanged among these differently sized cells. Thus, the increased INVQ size dramatically loads the slave latch, increasing its T, when the flip-flop cell size is increased.

Fig8. Normalized T_s and T_{eff} vs. cell sizes.

Fig8 shows for different flip-flop sizes. T increases almost linearly with the increase in cell size. Since is not affected by INVQ, the resulting based on (3) increases as well. In summary, the use of the smallest available flip-flops in the library is encouraged in order obtain

minimum T and maximum MTBF. This sometimes counter-intuitive guideline should be used for all library flip-flop cells in the synchronizer.

IV. Minimum routing between flip-flops

To achieve desired MTBF values, high speed synchronizers are usually built as pipelines of N flip-flops (Figure 9). From (1) the resolution time (S) is determined by [14]:

$$S = (N-1)\cdot(T_C - t_{CQ} - t_{pd} - t_{su}) \qquad (6)$$

where is the clock-to-Q propagation delay of each flip flop in the synchronizer, is the routing delay to the next flip-flop in the pipeline, is the setup time and is the clock period (= 1/ f_c). When is long compared to, and they can be neglected. However, when the receiving domain frequency is high, they should be taken into account. In order to increase to the maximum possible value, the IC designer needs to reduce the routing delay to a minimum. This can be achieved by imposing stringent constraints on these delays (Fig9) and by placing them closely together.

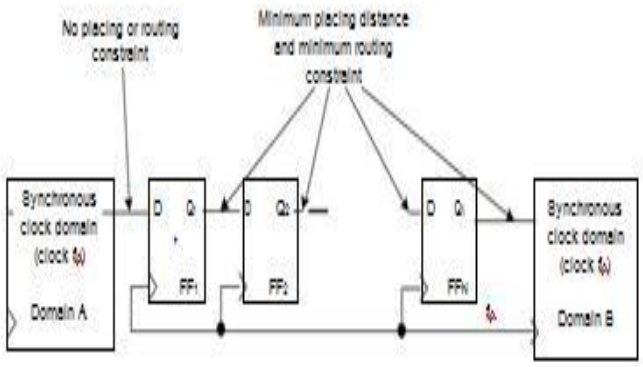


Fig9. Placing and routing constraints for multistage synchronizer.

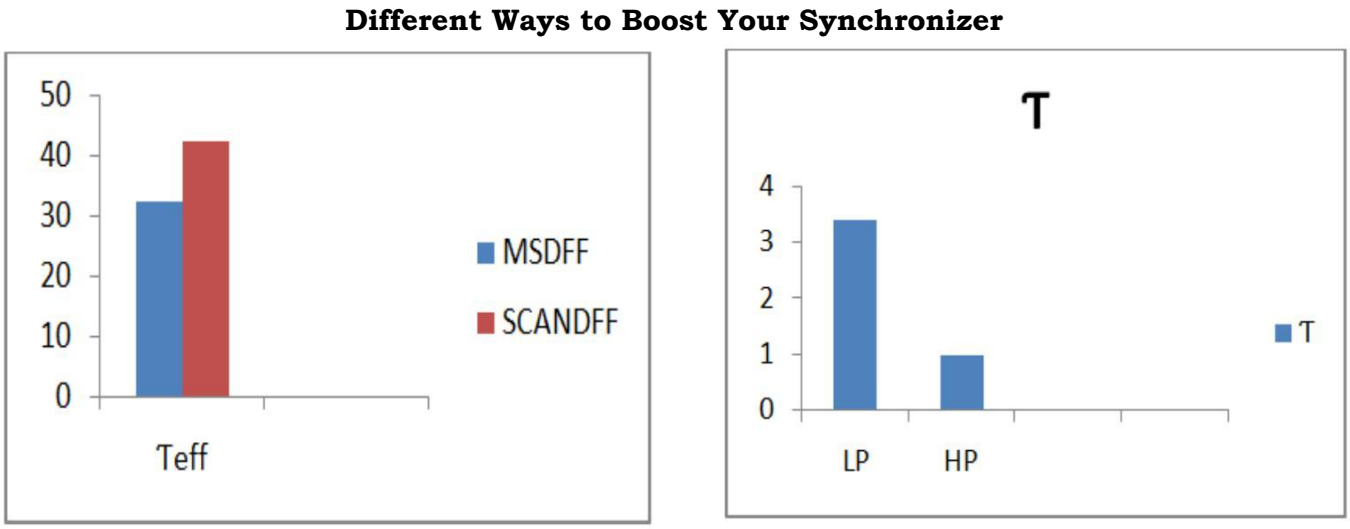


Fig10. Normalized Teff values.

B. Boosting the Process Technology I. Process flavor

The selection of the process technology to fabricate an IC has diverse criteria, power and performance being the most critical ones. Foundries provide a variety of process families tailored to different needs that are often denominated process flavors. The aim of this sub-section is to analyze the different flavors with respect to metastability performance. Process flavors differ in terminology and type depending on the vendor. A popular classification divides the technology node into low-power (LP) and high-performance (HP) flavors. However, in modern technologies, more detailed classifications are available. In [21] two classifications are added, the low-power-high-k metal gates (HPL) and the high-performance-for-mobile (HPM) flavors. In [22] three flavors are available, LP, high-performance-low-power (HLP) and HPM, while in [23] the denominations are super-low-power (SLP), low-power-high-performance (LPH) and high-performance-plus (HPP). Physical factors affecting the different flavors include nominal supply voltage, threshold voltage of the transistors, gate fabrication and stress memorization techniques (SMT). The exact „ingredients" behind each process flavor depend on the foundry vendor and are a combination of the above mentioned factors. The exact proportion of each factor is usually a carefully guarded secret. An additional important factor that influences future designs is the use of non-planar transistor architectures. We now analyze how each factor affects metastability parameters. The effect of supply voltage and threshold voltage on metastability is evaluated in separate sub-sections below since they can vary within the chip, due to multiple power domains on chip, or multi-threshold circuits within the same IC. The comparison has been performed under the same supply voltage and standard threshold voltage conditions. The results are normalized to the HP value. The LP flavor shows a T is higher compared to HP. This enormous difference cannot be neglected, especially when migrating circuits among different technology flavors. If the designer can choose the process flavor, HP is preferred from a maximum MTBF point of view.

Fig11. T values for different process flavours.

II. Minimum threshold voltage (Vth)

While traditionally a single level of transistor threshold voltage was available in the chip, as determined by the fabrication process, modern technologies offer a choice of a variety of threshold voltages for different transistors in the same IC. Multi-threshold CMOS (MTCMOS) technology has emerged as an increasingly popular technique to reduce leakage power in high performance ICs [5] [6]. The choice of which threshold voltage to use is a compromise between performance and power. Lowering the threshold voltage generates faster transistors (5) with higher leakage currents, while increasing the threshold reduces leakage but slows down the

transistors. In modern technologies the choice of V_{TH} is usually made among three of five predetermined values such as ultra-low, low, standard, high and ultra-high V_{TH}. As determined by (5), using low threshold transistors increases and reduces T. Three different threshold levels were simulated generating different values. The lowest value is achieved for the lowest V_{TH}. In summary, for the flip-flops forming the synchronizer, transistors with minimum V_{TH} are preferred in order to reduce T.

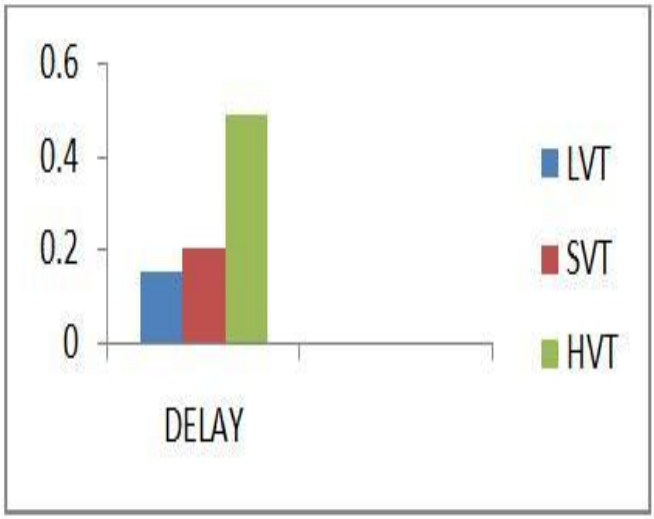


Fig12. Delay values for different threshold voltages.

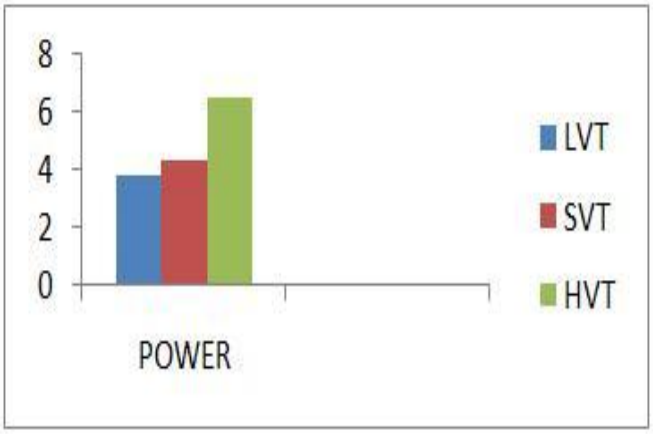


Fig13. Power Values for Different Threshold Voltages.

III. Supply Voltage

The selection of supply voltage is a significant system decision which directly determines performance and power of a circuit. As shown in[2],[3] supply voltage has a substantial effect on T. Supply voltage may vary within an IC due to different power domains on chip and also dynamically by means of techniques such as dynamic voltage scaling and due to IR drops. Figure 13 presents simulations of normalized T versus normalized supply voltage. When voltage is reduced by 15% from nominal V_{DD}, T increases more than 3.5 times its nominal value. This can be explained by means of (5): When V_{DD} is decreased, g_m decreases, which according to (4), generates an increase in T [24]. Hence, when the supply voltage is decreased for power considerations, the repercussion on MTBF should be considered. In summary the use of higher supply voltages is recommended when synchronization issues are critical.

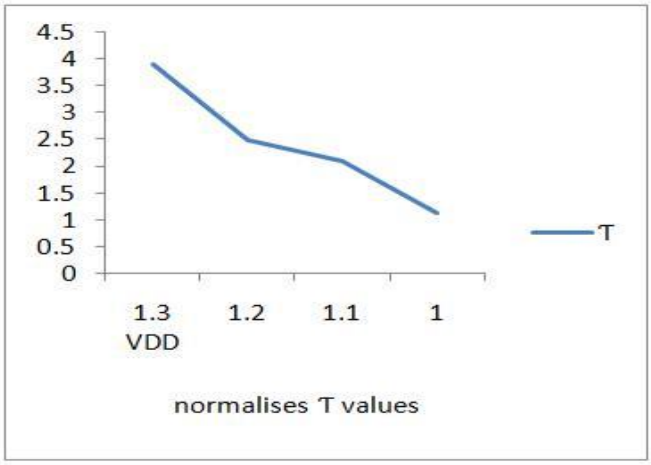


Fig14. T values for different supply voltages.

IV. Conclusion

In this project, guidelines and techniques to boost the performance of N-flip-flop synchronizers to realize minimum
τ and most MTBF is given. The trade-off between capacitance and transconductance within the synchronizer nodes that helpful to evaluate different aspects is described. The factors affecting metastability were divided into circuit, process and operating conditions, and boosting techniques for every factor is given. Global factors that affect the complete IC design guidelines that can be applied for individual synchronizers. For the global perspective, fabrication in high performance flavor technologies with the minimum threshold voltage allowed by the process is advocated. Increasing the supply voltage improves metastability resolution. The employment of scan and reset flip-flops should be avoided when possible to improve reliability. The minimum flip-flop cell size should be selected to boost τ.

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